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AMENDMENT TO THE CLAIMS

Please amend the claims as follows:

1. (previously amended) A method for converting at least one digital input signal to at least one analog representation signal thereof, comprising:
(a) feeding a DSP with said at least one digital input signal and a synchronization clock,
(b) repeatedly identifying a model of a digital to analog waveform converter for creating a representation of the relationships between said DSP digital outputs and at least one of said at least one analog representation signal, wherein said digital to analog waveform converter comprises discrete output devices and a MIMO system,
(c) said DSP is calculating n digital outputs, by using said at least one digital input signal and the identified model of said digital to analog waveform converter,
(d) said n digital outputs are received by k discrete output devices comprising in total: n digital inputs, m analog outputs, and simple conversion rules between said n digital inputs and said m analog outputs,
(e) said MIMO system receiving said m analog outputs, and providing at least one output analog signal equivalent to said at least one digital input signal.

2. (previously amended) The method of claim 1, wherein said MIMO system comprises low accuracy components featuring high bandwidth, high gain, and low current consumption.

3. (original) The method of claim 1, wherein said MIMO system comprises passive components.

4. (original) The method of claim 1, further comprising clock skew.

5. (original) The method of claim 1, wherein said MIMO system is time varying according to said synchronization clock.

6. (previously amended) The method of claim 1, wherein said identifying the model comprises identifying the inverse relation.

7. (previously amended) The method of claim 1, wherein said identifying the model comprises feeding at least one known digital signal to said at least one digital input

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signal in a training period, and reading said known digital signal and digital result from at least one analog to digital converter connected to said at least one analog representation signal, and identifying the model of said digital to analog waveform converter by applying a system identification algorithm.

8. (previously amended) The method of claim 7, wherein said at least one known digital signal comprises a sequence of independently and identically uniformly distributed pseudo-random numbers.

9. (previously amended) The method of claim 1, wherein said model is identified by applying an identification algorithm comprising a-priori statistical knowledge.

10. (previously amended) The method of claim 1, wherein said digital to analog waveform converter is enclosed in a system performing several signal processing functions which contain information regarding said at least one analog representation signal, and said information is sufficient for the step of identifying the model of the digital to analog waveform converter.

11. (previously amended) The method of claim 1, wherein an additional digital to analog waveform converter comprising a system model with unknown parameters is used for identifying said model of said digital to analog waveform converter, and unknown parameters of both models are identified by joint model identification algorithm.

12. (previously amended) The method of claim 11 where said joint model identification algorithm is based on feeding said digital to analog waveform converter with at least one known training sequence.

13. (previously amended) The method of claim 12, wherein said at least one known training sequence comprises an independently and identically distributed pseudo-random sequence.

14. (previously amended) The method of claim 1, wherein the step of identifying the model further comprises low speed components sampling said at least one analog representation signal every few samples and training only on the sampled samples.

15. (previously amended) The method of claim 1, wherein the step of identifying the model further comprises a low speed DAC reference, wherein a training digital signal is fed both to said low speed DAC reference and to said digital to analog waveform converter, and the analog output signals of the low speed DAC reference and said at

least one analog representation signal are subtracted in order to create an error signal; said error signal is sampled and fed to said DSP for training.

16. (previously amended) The method of claim 1, wherein said discrete output devices comprise at least one low resolution digital to analog converter.

17. (original) The method of claim 1, wherein the value of each of said m analog outputs is selected from a predefined group of values.

18. (original) The method of claim 1, wherein said m analog outputs are time varying according to a predetermined waveform.

19. (previously amended) The method of claim 1, wherein said MIMO system is selected from the group consisting of continuous MIMO system, MIMO system having a unified model, and continuous MIMO system having a unified model.

20. (previously amended) The method of claim 1, wherein the step of calculating the n digital outputs comprises inverting said model by using internal controller in order to keep the error to be within a deterministic or probabilistic set of predefined constraints and internal constructing device for implementing, in the digital domain, the mathematical equivalence of the transfer function of said digital to analog waveform converter.

21. (original) The method of claim 19, wherein said MIMO system is a linear MIMO system.

22. (cancelled)

23. (cancelled)

24. (previously amended) The method of claim 1, wherein said MIMO system is a linear MIMO system, and the step of identifying the model further comprises LMS technique.

25. (previously amended) A method comprising:

(a) feeding a DSP with at least one digital input signal and synchronization clock,

(b) occasionally or within a repetitive training period, said DSP is identifying a model of a digital to analog waveform converter wherein said digital to analog waveform converter comprises at least one discrete output device and m MIMO stages, and whereby the model represents the relationships between digital outputs of said DSP and at least one analog output signal of the m MIMO stages,

(c) calculating n digital outputs, by using said at least one digital input signal and the identified model,

(d) said n digital outputs are received by said at least one discrete output device comprising, in total, n digital inputs, m analog outputs, and simple conversion rules between said n digital inputs and said m analog outputs,

(e) corresponding MIMO stage to each one of said m analog outputs, excluding first MIMO stage, are receiving at least one analog input signal from the preceding stage and the appropriate analog signal said at least one discrete output device; first MIMO stage is receiving only the appropriate analog signal from said at least one discrete output device; all m MIMO stages are providing at least one output analog signal; last MIMO stage is providing at least one output analog signal equivalent to said digital input signal.

26. (previously amended) The method of claim 25, wherein each of said m MIMO stages comprises attenuating the signal, and adding a predefined constant or subtracting said predefined constant from said attenuated signal, according to said DSP decision.

27. (cancelled)

28. (original) The device of claim 55, wherein said analog representation having RMS below 10 mili volt at frequency above 10 MHz.

29. (cancelled)

30. (original) The device of claim 55, wherein said synchronization clock is a signal selected from the group consisting of fixed pulse shape and frequency, and any deterministic signal featuring frequency.

31. (cancelled)

32. (cancelled)

33. (cancelled)

34. (previously amended) The device of claim 55, wherein said DSP is implemented by two separate DSPs.

35. (previously amended) The device of claim 55, wherein said training generator is implemented within said DSP.

36. (cancelled)

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37. (previously amended) The device of claim 55, wherein said device is enclosed in a system performing several signal processing functions which contains information regarding said at least one analog representation signal, and said information is sufficient for identifying the model.

38. (previously amended) The device of claim 55, further comprising an additional digital to analog waveform converter comprising a system model with unknown parameters, whereby said additional digital to analog waveform converter is used for identifying said model, and unknown parameters of both models are identified by joint model identification algorithm.

39. (previously amended) The device of claim 55, further comprising low speed components, whereby said low speed components are sampling said at least one output analog signal every few samples and training only on the sampled samples.

40. (previously amended) The device of claim 55, wherein said discrete output devices further comprising at least one low resolution digital to analog converter.

41. (previously amended) The device of claim 55, wherein said MIMO device is selected from the group consisting of continuous MIMO device, MIMO device having a unified model, and continuous MIMO device having a unified model.

42. (previously amended) The device of claim 41, wherein said MIMO device is a linear MIMO device.

43. (previously amended) The device of claim 55, wherein said device is implemented as a multi-stage configuration.

44. (previously amended) The device of claim 55, wherein said device is implemented as a multi-stage configuration and said multi-stage configuration further comprising an iterative control, whereby said iterative control is transferring a residual error to subsequent stages in each stage where the control function is successfully implemented.

45. (currently amended) A multi-stage digital to analog waveform converter comprising stages, wherein each stage comprises:

(a) amplifier amplifying an input ~~digital~~ signal,

(b) means for approximately integrating the amplified ~~digital~~ signal,

(c) ~~means~~ for a clock for synchronizing said ~~multi-stage digital~~ signals ~~constructor~~ stage,

(d) means for adding at least one predefined correction to said amplified ~~digital~~ signal, wherein multi-stage digital to analog waveform converter further comprising digital signal processing means calculating said corrections by utilizing the relationships between the corrections and at least one of the amplified signals.

46. (currently amended) The device of claim 45, wherein ~~said~~ analog output signal of said waveform converter having RMS below 10 mili volt at frequency above 10 MHz.

47. (original) The device of claim 45, wherein said amplifier is open loop transconductance amplifier.

48. (currently amended) The device of claim 45, wherein said ~~means for synchronizing to a~~ clock is ~~comprises switching~~ modulating said amplifier ~~according to a clock~~.

49. (currently amended) The device of claim 45, wherein said digital signal processing means ~~means for comparing the integrated amplified digital signal with a threshold~~ comprising a training generator feeding at least one known digital signal to said input digital signal in a training period, and reading said known digital signal and digital result from at least one ADC connected to said at least one analog output signal, and identifying the model of said multi-stage digital to analog waveform converter by applying a system identification algorithm.

50. (original) The device of claim 49, wherein said training generator is implemented within said DSP.

51. (currently amended) A parallel multi-stage digital to analog waveform converter, comprising:

(a) plurality of digital to analog waveform converters receiving at least two different digital input signals,

(b) said plurality of digital to analog waveform converters are placed on the same silicon substrate, featuring crosstalk between themselves ,

(c) a common DSP, whereby said DSP is treating said crosstalk effect,

whereby each of the plurality of the digital to analog waveform converters comprises: amplifier amplifying an input ~~digital~~ signal, integration means for integrating the amplified ~~digital~~ signal, means for adding predefined corrections to the amplified signal, a synchronization clock~~, and a comparator~~.

52. (previously amended) A method comprising:

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(a) feeding a DSP with said at least one digital input signal and a synchronization clock,

(b) calculating, by said DSP, n digital outputs, by using said at least one digital input signal and a digital to analog waveform converter model,

(c) receiving by k discrete output devices said n digital outputs; said k discrete output devices comprising, in total, n digital inputs, m analog outputs, and simple conversion rules between said n digital inputs and said m analog outputs,

(d) receiving by a MIMO system said m analog outputs, and providing at least one output analog signal equivalent to said at least one digital input signal.

53. (previously amended) The method of claim 52, wherein said MIMO system can be considered as time invariant by using analog or digital compensation methods.

54. (previously amended) The method of claim 7, wherein said analog to digital converter and said digital to analog waveform converter are adaptive and trained together.

55. (previously amended) A device comprising:

(a) a digital to analog waveform converter comprising: (i) at least one discrete output device and (ii) a MIMO device; said discrete output device comprising simple conversion rules between said digital inputs and said analog outputs; said discrete output device is connected to said MIMO device; and said MIMO device comprising at least one analog input and at least one analog output;

(b) A DSP connected to at least one digital input signal, a synchronization clock and at least one discrete output device, whereby said DSP, occasionally or within a repetitive training period, is identifying a model of said digital to analog waveform converter for creating a representation of the relationships between said digital outputs of said DSP and at least one of the analog output signals of said MIMO device; whereby said DSP while not in training mode is calculating the appropriate input to the at least one discrete output device using said model to provide at least one output analog signal equivalent to said digital input signal.